classify a destination access as a targeted storage group according to information in a destination address field of the one or more instructions executed on the processor; and

evaluate the classified destination address based on whether the instruction updates the targeted storage group.

36 35

8. (New) The context switch controller of claim 7, wherein

the dirty bit logic is responsive to a context switch by saving the storage groups based on the evaluation of the classified destinations.

6 et

37 34

9. (New) The context switch controller of claim 6, wherein the data storage unit is configured to hold data operated by the one or more instructions executed on the processor.

end

38 34

10. (New) The context switch controller of claim 6, wherein each one of the plurality of storage groups comprises one or more storage elements.

REMARKS

Claims 1-5 are pending in the application and have each been rejected on various double patenting grounds. New claims 6-10 have been added.

Per Examiner's request, figure 1 is being resubmitted. No new matter has been added.

Rejections under 35 USC §101

Claims 1-4 have been rejected under 35 USC 101 as claiming the same invention as that of claims 1 and 11-12 of prior U.S. Patent No. 6,205,543. Applicants respectfully traverse these rejections.

In rejecting claim 1, Examiner apparently reasons based on perceived correspondence of one particular claim but does not actually consider the elements of claim 1. Further, the Examiner has not provided the necessary literal infringement analysis required to establish a prima facie case for same-invention double patenting.